ABSTRACT OF THE DISCLOSURE

A control method of a semiconductor memory device which enables control of an operation mode including an operation that might become a noise source by using an operation mode including an operation from which the influence of noise should be eliminated, and a semiconductor memory device are provided. First and second operation sections performing independent operations are provided, and a signal output section for outputting a second signal S2 and a mode controller section for supplying a control signal C1 are provided in the second operation section. The control signal C1 is outputted from the mode controller section and the signal output section outputs the second signal S2 to a memory cell array, thus performing a second operation. A predetermined first signal SS1 is supplied to the signal output section from the first operation section, thus delaying an output response of a predetermined second signal. While the control signal C1 is outputted from the mode controller section, the supply of the predetermined second signal to the memory cell array can be delayed. The influence of state transition in the second operation on the operation state of the first operation can be eliminated.